Hall Ticket Number:

Code No.: 22315 AS

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (E.C.E.) II Year II-Semester Advanced Supplementary Examinations, June/July-2017

Pulse, Digital and Switching Circuits

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Show that a Lowpass RC circuit acts as an integrator.
2. Mention the effects of diode characteristics on clamping voltage.
3. Compare conventional Bi-stable Multi-vibrator and Schmitt trigger circuits.
4. Sketch all the wave forms of collector coupled Mono-stable Multi-vibrator when it is in stable and quasi stable state.
5. Realize EX-OR and EX-NOR gates using minimum number of NAND gates.
6. Implement a half adder with two 2x1 multiplexers and NOT gates.
7. Write the function for the carry outputs of each stage of a four bit Carry Look Ahead adder.
8. Construct JK Flip flop using D flip flop, a 2 to 1multiplexer and an inverter.
9. Differentiate among Synchronous and Asynchronous sequential circuits.
10. A machine has to detect a sequence 1010, obtain its state diagram. (over lapping allowed).

Part-B (5 × 10 = 50 Marks)

11. a) Explain the operation of an RLC circuit when a step input is applied at its inputs (with initial condition equal to be zero) as a function of K. [5]

    b) The limited ramp is applied to an RC differentiator as shown in fig. 11 b. Draw to scale the output wave form for the cases T = RC, T = 0.2 RC & 5 RC. [5]

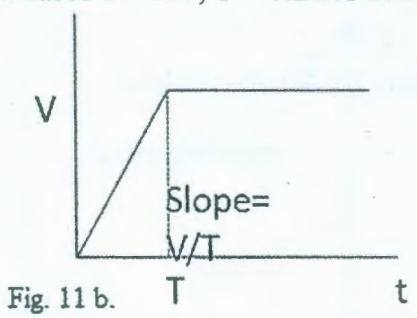

Fig. 11 b.

12. a) Derive an expression for gate / pulse width of an emitter coupled Mono-stable Multi-vibrator. [4]

    b) Describe the operation of a Schmitt trigger circuit and derive expressions for UTP and LTP. [6]

13. a) Express the compliment of the following function in product of sum form F(A,B,C,D) = ∑(3,5,9,11,15). [3]

    b) Draw a logic diagram using only two input NOR gates to implement the following function f(A,B,C,D) = (A XNOR B) (C XOR D). [4]

    c) Implement the Boolean function F(A,B,C,D) = ∑(1,3,4,11,12,13,14,15) using Multiplexer. [3]

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14. a) Reduce the given state diagram and perform state assignment. [6]

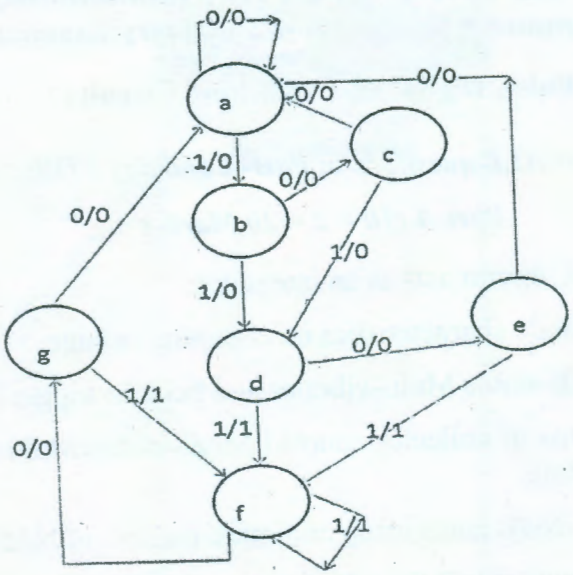

Fig. 14 a.

b) Draw the truth table of priority encoder and differentiate it with normal encoder. [4]

15. a) Design 4-bit UP/DOWN counter. Use one control signal to select either to perform UP counting or DOWN counting. Mealy type of modelling and JK flip-flops has to be used. [6]

b) Draw the block diagram of universal shift register. [4]

16. a) Explain about linear and non-linear wave shaping circuits. [5]

b) Design a sweep circuit using UJT to trigger TRIAC. [5]

17. Write short notes on any *two* of the following: [5]

a) Static Hazards [5]

b) Ring counter [5]

c) Designing procedure for Mealy machine.